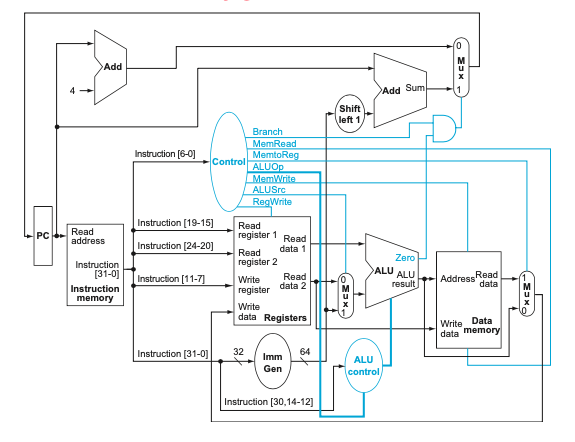
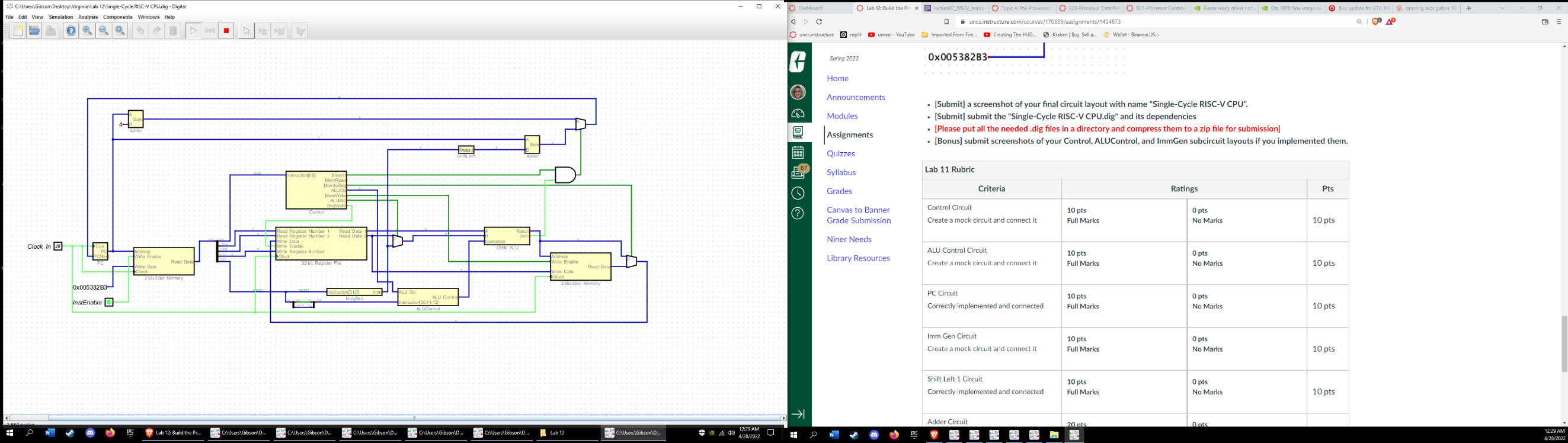
**Single-Cycle RISC-V CPU**

**Based on the image**

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\*Control, ALUControl, and ImmGen subcircuits implemented