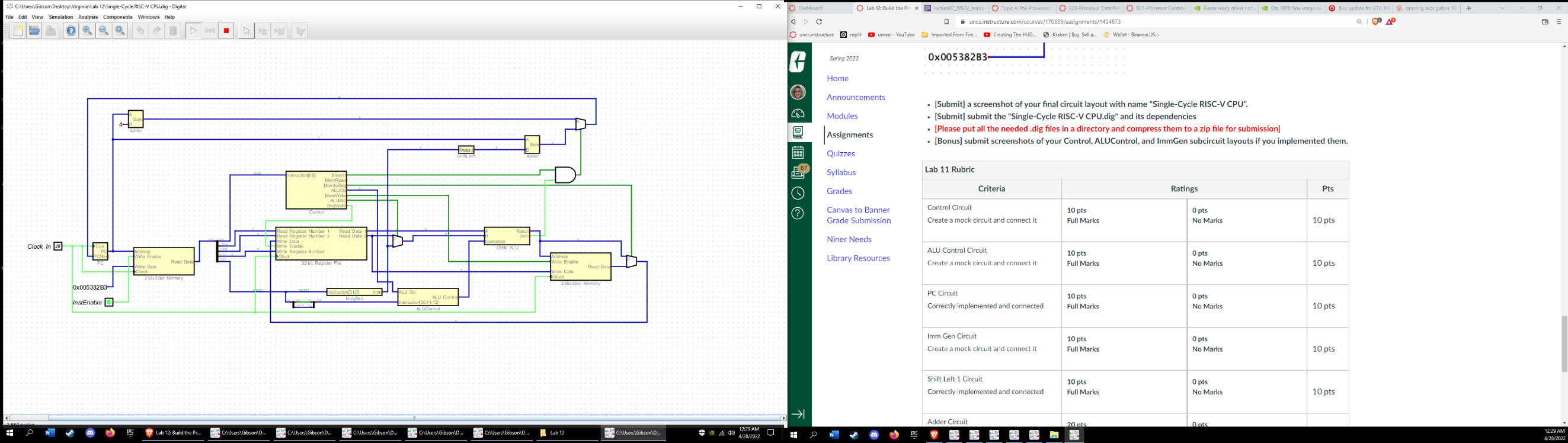
**Single-Cycle RISC-V CPU**

\*Control, ALUControl, and ImmGen subcircuits implemented